EIPC-3

ELTEC Industrial PC

Hardware Manual

Revision 1A

ELTEC
elektronik mainz

Revision History

Revision	Changes	Date
1A	First Edition, valid for Hardware revision 3A,	25.06.01 ar

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1 Specification

1.1 Main Features

- Fully AT-compatible industrial PC
- Socket 370 CPU for Celeron/Pentium III CPU up to 850 MHz, 66/100 MHz FSB.
- PICMG compatible board design with PCI and ISA slot connectors
- 2 DIMM sockets for up to 512 MB SDRAM
- 256 KB on-chip second level cache, depending on CPU
- PCI local bus, 32-bit, 33MHz
- USB/IrDA port Option
- AGP Graphics controller with 2MB video RAM supports simultaneous CRT and flatpanel display
- PCI UltraWide SCSI controller, supports up to 40MB/sec (UltraWide SCSI)
- Integrated EIDE hard disk controller, supports 2 independent IDE channels
- PCI 10/100 Mb/s Ethernet controller (10BaseT / 100BaseTX), optional Boot ROM
- PCI-PCI Bridge, support up to 4 external PCI-Busmaster on a PICMG compatible backplane
- Two serial channels with hardware handshake
- Bi-directional parallel printer port (EPP/ECP)
- Keyboard and mouse interface with PS/2 style connectors
- Watchdog timer, can be enabled after system boot

- Power saving functions
- ESD and EMC protection for all front panel I/O, meeting the CE requirements

1.2 General Descrption

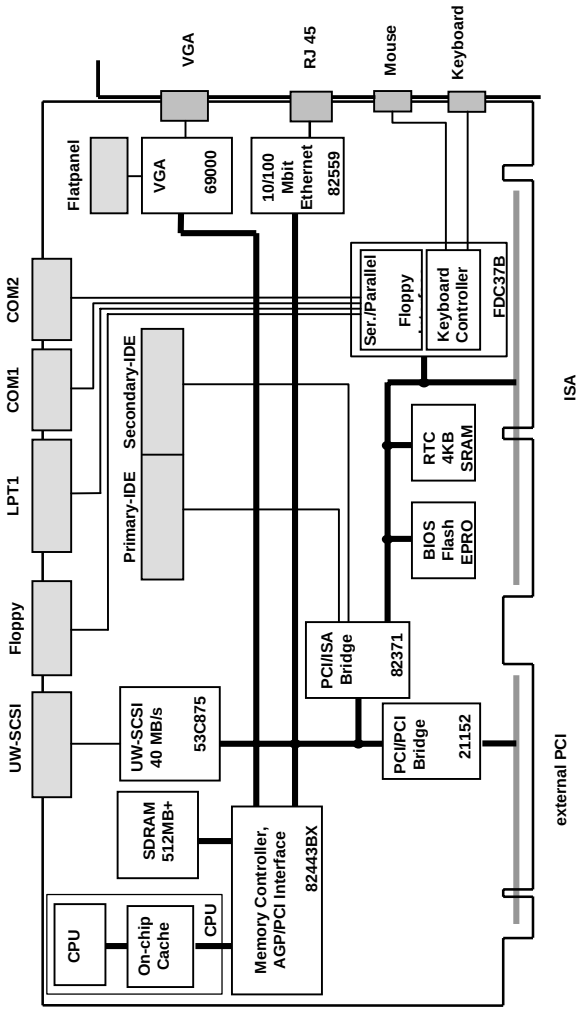

Figure 1—1: Block Diagram

The EIPC-3 is a fully AT compatible PC for industrial application. The standardized PCI slot CPU format (PICMG) permits intallation in a industrial PC housing. Equipped with an Pentium III® processor it meets the performance requirements of modern software. Unlike off-the-shelf PCs the EIPC-3 is designed for rugged environments. Special care has been taken to achieve a maximum use of extendability for customized applications.

Different types of frequencies and processors are supported by the EIPC-3. The clock frequency ranges from 300 to 850 MHz and more. In contrast to EIPC-2 the EIPC-3 support Celeron/Pentium III processor with 100 MHz Front Side Bus to archieve the maxium performance of the chipset.

Up to 512 MB of DRAM are available for large application software and data. Standard 168-pin DIMM modules are used. To reduce system costs the customer can select the right amount of memory needed for the application. Updates of memory resources are possible if required.

The backbone of the EIPC-3 is the synchronous, 32-bit PCI local bus. It runs at halfthird the CPU bus frequency, typically 33 MHz. Although data and addresses are multiplexed a maximum data transfer rate of 133 MB/sec can be achieved during bursts. The CPU communicates with all I/O devices via PCI. To reduce the load on the PCI, the CPU use the AGP bus to communicate with the graphic controller.

I/O devices which require a high data throughput to the CPU or main memory are placed directly on the PCI bus. I/O devices which are less time critical are connected to the commonly used ISA bus. A single chip bridge links PCI and ISA bus together. The bridge contains a posted write buffer for PCI initiated memory write cycles to the ISA bus to relieve the PCI bus from waiting for the end of an ISA write cycle. A similar functionality is provided with an ISA-to-PCI buffer which collects both write and read cycles from ISA masters and DMA channels.

Because today's graphics applications require a high data throughput, the graphics controller is connected to the AGP bus. It does not only feature the older VGA graphics standards but also provides high resolution screens. With 2 MB of video RAM highest possible screen resolutions are 1024 x 768 pixels with 64k simultaneously displayed color. Smaller resolutions can be used in true-color mode. To achieve higher data rates the video memory can be addressed in a linear mode in spite of the commonly used memory mapping techniques. A Windows accelerator provides additional performance in Windows application. The video outputs support both CRT and flat panel displays. A wide range of display types can be adapted to the Eltec-IPC. Displays can be connected using unbuffered TTL signal level.

The EIPC-3 supports up to 4 IDE devices (2 ports) with up to 33 MB/sec (UltraDMA/33) as well as an 16 bit SCSI-I and II interface at the PCI local bus where up to 15 devices can be connected. The controller support UltraSCSI with transfer rates up to 40 MB/sec if supported by the devices.

To achieve maximum flexibility and performance the Eltec-IPC has equipped with a PCI-PCI bridge DEC 21152 to support up to 4 PCI-Busmaster on a external PICMG compatible backplane. The bridge is fully compilant with PCI Local Bus Specfication 2.1. It provides full support for delayed transactions, which enables the buffering of memory read, I/O, and configuration transactions.

The network interface consists of a Intel 82559 PCI. The controller is capable of detecting the used network data rate (10 / 100 Mbit) or can be configurated to operated at a fixed rate. The network is connected via a twisted pair connector (10BaseT/100BaseTx) at the frontpanel. A set of LED are provided to show the state of the network. If desired, a net boot EPROM can be used for diskless stations.

All other PC compatible I/O devices reside on the ISA bus of the EIPC-3. Two serial channels with hardware handshake (COM1, COM2) and one bidirectional parallel port (LPT1) are available at

the front panel. The serial port devices are compatible to NS16450 and NS16550 and have internal FIFOs for high-speed modem support. The parallel port is Centronics compatible but supports also EPP and ECP mode.

The keyboard controller features an AT compatible keyboard interface. PS/2 compatible mice are supported via a separate connector at the frontpanel.

The Eltec-IPC is equipped with a floppy controller which supports the 5 ¼" and 3 ½" disk sizes. Floppy disks with up to 2.88 MB density can be used.

The BIOS Flash EPROM has a size of 256KByte. It contains the main BIOS and the BIOS extension for SCSI und Graphics. It is incircuit programmable for BIOS updates.

The Eltec-IPC is equipped with one integrated DC/DC converter for CPU core voltage (automaticaly detzeczed) and all circuitries requiring 3.3 V or 2.5 V voltage. Because the voltages are generated from 5 V no special power supply has to be provided by the customer.

The PICMG compatible PCI-ISA card edge connector allow the use of PICMG backplane to increase the functionality of the EIPC-3.

1.3 Technical Details

1.3.1 CPU

All Socket 370 processors with 66 or 100 MHz FSB are supported by the EIPC-3. Therefore it is possible to scale the system depending on requested performance. Equipped with a 850/100 MHz Pentium III processor you obtain maximum performance with an performance index of 164 SYSmark2000. (For comparison: Celeron 366/66 MHz 72 SYSmark200)

1.3.2 Chipset

The EIPC-3 is based on the Intel 440BX PCI chip set, the reference for Pentium III and Celeron chip sets. Also, availability for longer periods than what is common in the PC market is guaranteed. The BX chipset consists off two chips: First the Northbridge (82443) which contains CPU-, Memory-, AGP- and PCI-Interface and second the Southbridge containing PCI-ISA Bridge, IDE-Interface, Realtime Clock and CMOS-Memory.

1.3.3 Memory Configuration

The 64-bit wide memory allows configurations from 32 MBytes to 256 MBytes and more (t.b.d.) using two DIMMs with 66-MHz or 100 MHz SDRAMs (100 MHz SDRAM are required for processors with 100 MHz FSB). The memory size is detected automatically.

1.3.4 Firmware

The BIOS is stored in a Boot-Block Flash-EPROM which enables easy BIOS updates. Boot from floppy, IDE, SCSI, CD, LS-120 is supported. A net boot EPROM can be installed on a socket.

1.3.5 Graphics Interface

The graphics interface of the EIPC-3 is a AGP-based graphics controller C&T 69000, which achieves superior performance through the 32-bit interface to the AGP. CRT monitors and flat panel display technologies including plasma, EL, LCD are supported.

The resolution ranges up to 1280 x 1024 pixels at 256 colors and 75 Hz. TFT LCD panel are supported. With resolutions of up to 1280 x 1024 pixels simultaneous displays of CRT and flat panels are possible. The graphics controller provides logic for power-saving functions for flat panels.

The graphic interface is fully compatible with the VGA standard at the hardware, register and BIOS level. Mode initialization is supported at the BIOS and register levels ensuring compatibility with all application software.

1.3.6 Floppy Disk

All types of common 3,5" and 5,25" Floppy drives are supported.

1.3.7 Hard Disks

Hard Disks are supported by the PCI-based EIDE port with Ultra DMA/33 transfer and the Ultra-wide SCSI port with 40 MB/sec transfer rate.

The IDE interface (Integrated Device Electronics) is part of the Intel chipset. That means that the IDE controller is directly connected to the PCI bus, achieving higher data rates than with ISA based controllers.Up to four IDE devices can be connected.

The SCSI interface is built with a 53C875 controller chip from LSI Logic (former Symbios Logic). It is directly connected between PCI and SCSI bus. A PCI bus master DMA channel and an internal SCRIPT processor leaves the processor free from doing time expensive data transfers. DMA transfers operate in burst mode on the PCI bus for best performance. SCSI-I and II protocol is supported. With 16-bit SCSI bus size a data transfer rate of either 20 MB/sec in asynchronous or 40 MB/sec in synchronous mode (UltraWideSCSI) can be achieved. The BIOS contains special firmware to support boot and BIOS routines. After the operating system was booted a SCSI harddisk behaves like an IDE harddisk. Up to fifteen SCSI devices can be connected to the bus.

1.3.8 Ethernet Interface

The network interface uses the network controller Intel 82259 for 10/100 Mb connectivity with 10BaseT (twisted pair) or 100Base TX connectivity. The 82259 has an integrated IEEE 802.3 10BASE-T and 100BASE-TX compatible transmitter for reducing system cost. A set of LEDs are provided to show the state of the network (see Fig. 2–1).

1.3.9 I/O Features

Two asynchronous 16550 compatible serial channels with up to 115 kbaud transfer rate and 16-byte FIFO with RS232 levels are available. Printers can be connected to a fully bidirectional parallel port supporting IEEE 1284 enhanced modes (EPP and ECP). PS/2-compatible keyboard and mouse interface are provided. A USB port is available for connecting to keyboard/mouse/scanners etc. For IrDA-Application one serial port of the EIPC-3 can be set to support this feature – There is no IrDA-Hardware (IR-Transmitter) on the board. Please contact ELTEC for USB and IrDA support.

1.3.10 Extended PCI Capabilities

The EIPC-3 contains two PCI busses which are connected through the PCI-PCI bridge. The first PCI bus (called internal, PCI bus 0) connects the onboard PCI devices (Ethernet, SCSI, PCI-ISA bridge and PCI-PCI-Bridge) to the Host-Bridge. The second one (called external, PCI bus 1) connects the devices on the PICMG backplane to the internal PCI bus.

The connection between the internal and external PCI bus is established by a 21152 PCI-PCI Bridge from Intel. It provides a complete secondary PCI bus interface without the need for additional components. To increase performance the 21152 has separate posted write, read data, and delayed transaction queues with significantly more buffering capability than first-generation bridges. In addition, the 21152 supports buffering of simultaneous multiple posted write and delayed transactions in both directions. The 21152 has sufficient clock and arbitration pins to support four PCI bus master devices directly on its secondary interface. The 21152 allows the two PCI buses to operate concurrently. This means that a master and a target on the same PCI bus can communicate while the other PCI bus is busy. This traffic isolation may increase system performance in some special applications.

1.3.11 CE Conformity

All I/O-signals routed to the front panel are filtered by special EMC filters to meet EMC requirements (class A).

1.3.12 Watchdog

The EIPC-3 has an on-board watchdog for operator-less environments.

1.3.13 Operating Systems

The software support for the EIPC-3 includes all standard PC software such as: Windows 98, Windows NT, DOS. Support for additional operating systems is in preparation.

1.3.14 Compatibility

The EIPC-3 is compatible to the EIPC with the following exceptions: CPU kernel (incl. memory) changed, SCSI and Ethernet changed and USB added.

1.4 Temperature/Power Specifications

1.4.1 Environmental Conditions

- Storage Temperature:0° C - 70° C
- Operating Temperature:0° C - 45° C (2 m/s forced air cooling)
- Cooling requirements for different environments and CPU frequencies should be discussed with ELTEC.
- Maximum Operating Humidity: 85 % relative

1.4.2 Power Requirements (without AGP, PCI or ISA extensions)

9A max.7A typ.at+5VDC±5 % (for the 850 MHz version)

200mA max.160mA typ.at+12VDC±10 %

100mA max.30mA typ.at-12VDC±10 %

MTBF Values

- tbd hrs (computed after MIL-HDBK-217E)
- Operating Temperature:0° C - 45° C

Ordering Information

Hardware:

Pentium III 600 MHz,

Graphics, EIDE, SCSI,

10BaseT/100BaseTX

Related Products:

- DSTN-Adapter for Sharp LM80c312 B-EIPC-800A
- Hardware Documentation
- BIOS Documentation

2 Interface Connectors

2.1.1 PICMG Connector

The PICMG connector consist of a PCI and a ISA connector. Please refer to [1] for more details about PICMG Specification.

2.1.2 Parallel Port

The bidirectional parallel port supports IEEE 1284 (ECP, EPP). The parallel port connector is part of the the additional frontpanel coming with the EIPC-3. It is also possible to mount these connector into a appropriated hole in the PC housing.

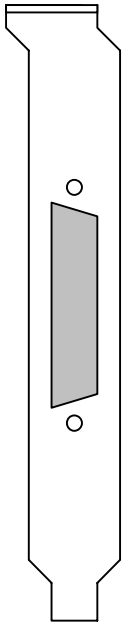

Figure 2—1: Location Parallel Port

Table 2—1: Pinout Parallel Port LPT1

Pin	Signal	Function
1	/STROBE	Strobe
2	D0	Data bit 0
3	D1	Data bit 1
4	D2	Data bit 2
5	D3	Data bit 3
6	D4	Data bit 4
7	D5	Data bit 5
8	D6	Data bit 6
9	D7	Data bit 7
10	/ACK	Acknowledge
11	BUSY	Busy
12	PE	Paper end
13	SELECT	Select
14	/AFD	Auto feed
15	/ERROR	Error
16	/INIT	Initialize
17	/SELECTIN	Select input
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	GND	Ground
25	GND	Ground

2.1.3 Serial

The EIPC-3 supports two serial ports accessible via a seperate frontpanel. Like the parallel port you can mount these connectors into the PC housing.

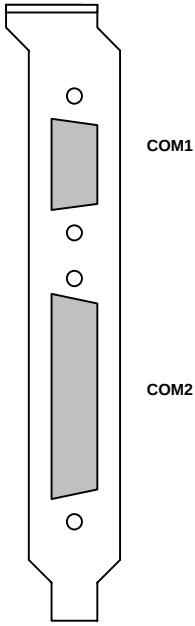

Figure 2—2: Location Serial Port

Table 2—2: Pinout Serial Port COM1 and COM2

COM1 (9 pin SUB-D)		
Pin	**Signal**	**Function**
1	DCD	Data Carrier Detect
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Ground
6	DSR	Data Set Ready
7	RTS	Ready to Send
8	CTS	Clear to Send
9	RI	Ring Indicator

COM2 (25 pin SUB-D)		
Pin	**Signal**	**Function**
2	TXD	Transmit Data
3	RXD	Receive Data
4	RTS	Ready to Send
5	CTS	Clear to Send
6	DSR	Data Set Ready
7	GND	Ground
8	DCD	Data Carrier Detect
20	DTR	Data Terminal Ready
22	RI	Ring Indicator
23..25		Not connected

2.1.4 Ethernet

The ethernet connector resides on the EIPC-3 frontpanel

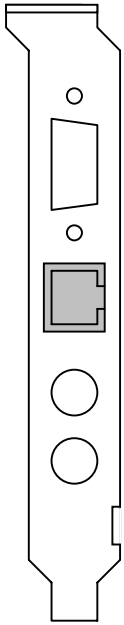

Figure 2—3: Location Ethernet Port

Table 2—3: Pinout Ethernet Connector

Pin	Signal	Function
1	TD+	Transmit data positive
2	TD-	Transmit data negative
3	RD+	Receive data positive
4		not connected
5		not connected
6	RD-	Receive data negative
7		not connected
8		not connected

2.1.5 Keyboard/Mouse

Like the EIPC the EIPC-3 has different PS/2 connectors for mouseand keyboard.

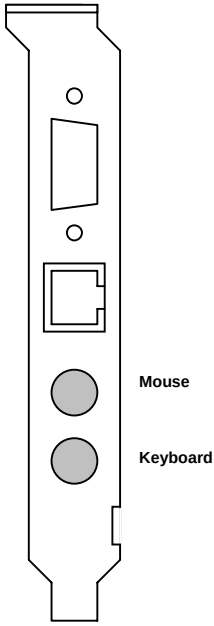

Figure 2—4: Location Keyboard/Mouse Port

Table 2—4: Pinout Keyboard Connector

Pin	Signal	Function
1	KBDAT	Keyboard Data
2	nc	Not connected
3	GND	Ground
4	5 V	Vcc
5	KBCLK	Keyboard Clock
6	nc	Not connected

Table 2—5: Pinout Mouse Connector

Pin	Signal	Function
1	MSDAT	Mouse Data
2	nc	Not connected
3	GND	Ground
4	5 V	Vcc
5	MSCLK	Mouse Clock
6	nc	Not connected

2.1.6 VGA Connector

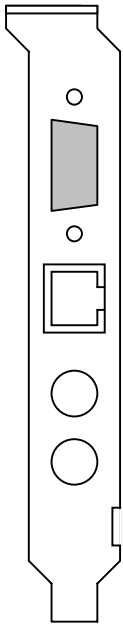

Figure 2—5: Location VGA Port

Table 2—6: Pinout VGA Connector

Pin	Name	Function
1	RED	Red channel
2	GREEN	Green channel
3	BLUE	Blue channel
4	nc	not connected
5	GND	Ground (digital)
6	GND	Ground (red)
7	GND	Ground (green)
8	GND	Ground (blue)
9	nc	not connected
10	GND	Ground (digital)
11	nc	not connected
12	DDC DATA	Monitor data
13	HSYNC	Digital HSync
14	VSYNC	Digital VSync
15	DDC CLK	Monitor data

Table 2—7: Pinout Flatpanel Connector

Pin	Signal	Signal	Pin
1	GND	FP(14)	**2**
3	CLK	GND	**4**
5	GND	GND	**6**
7	LP	FP(0)	**8**
9	FLM	FP(1)	**10**
11	GND	FP(2)	**12**
13	GND	GND	**14**
15	GND	FP(3)	**16**
17	FP(16)	FP(4)	**18**
19	FP(17)	FP(5)	**20**
21	FP(18)	FP(6)	**22**
23	GND	ENAB	**24**
25	FP(19)	nc	**26**
27	FP(20)	VDD (3.3 / 5V)	**28**
29	FP(21)	VDD (3.3 / 5V)	**30**
31	FP(22)	FP(23)	**32**
33	GND	ENA_VDD	**34**
35	GND	GND	**36**
37	FP(8)	FP(15)	**38**
39	FP(9)	FP(17)	**40**
41	FP(10)	reserved	**42**
43	GND	ENA_VEE	**44**
45	FP(11)	reserved	**46**
47	FP(12)	ENA_BKL	**48**
49	FP(13)	+12V	**50**

Note: Function of FP(0:23) depends on the graphic controller settings. See Chapter X.X for LCD settings

Attention: Cable length above 40 cm / 15“ may cause picture disturbance.

2.2 Definition of Board Parameters

2.2.1 AGP Bus

CPU to Graphic Accelerator:

Max. 528 MB/s (peak)

Bus Clock:

66.6 MHz (PCI x2)

2.2.2 PCI Local Bus

CPU to PCI Transfer Options:

Write post buffer

Max. 120 MB/s (peak)

PCI to Memory Transfer Options:

Max. 120 MB/s (peak)

Clock Speed:

33.3 MHz at 66.6 MHz CPU bus frequency

IRQs:

Four PCI interrupts rerouted to selectable ISA interrupts

2.2.3 ISA Bus

Bus Clock:

8.33 MHz at 33.3 MHz PCI frequency

Interrupt Capabilities:

IRQ(3-7, 9-12, 14-15)

DMA Channel Capabilities:

DMA slave or master mode

DMA (0, 3, 5, 6, 7)

2.2.4 Network

10BaseT / 100BaseTx (twisted-pair)

Transfer Speed:

max. 10/100 Mbit/s

2.2.5 SCSI

SCSI-I and II Ultra (8/16 bit)

Transfer Speed:

asynchronous transfer 5 MB/s

synchronous transfer 20 MB/s (8-bit)

synchronous transfer 40 MB/s (16-bit).

2.2.6 Serial I/O

2 Channels:

Full duplex, asynchronous

50 b/s - 115,2 KB/s

RS232 level

2.2.7 USB

One port:

1.5 / 12 Mb/s

Supply current for external devices: 500 mA.

2.2.8 IrDA

One port, alternate use for COM2

IrDA 1.0: 115.2 kbps @ 1m (3feet)

IrDA 1.1: 4Mbps @ 1m (3feet)

2.2.9 Keyboard:

MF2/AT mode

PS/2 mode

2.2.10 Mouse

PS/2 mode

Serial mouse at channel 1 or channel 2

2.2.11 Parallel I/O

Centronics bidirectional, unbuffered TTL

Transfer Rate: max. 2 MB/s

2.2.12 Video I/O

Dotclock: max. 135 MHz

CLUT: 4/8/16/24 bit/pixel

16, 256, 32 K, 64 K, 16 M colors depending on screen resolution

Video Resolution: 320 x 200 - 1280 x 1024

Horizontal Frequencies: max. 80 kHz

Vertical Frequencies: max 85 Hz

2.2.13 MTBF Values:

8356 h (computed after MTL HDBK-217E)

111970 h (realistic value from industry standard experience)

ESD Values:

2 kV (Human body method)

2.2.14 Environmental Conditions

Storage Temperature: 0 ºC - 70 ºC

Table 2—8: Operating Temperature

CPU Frequency (MHz)	CPU Power Dissipation (W)	Air Temperature (º C) (T_A)	Air Flow (m/s)	Heat Sink	Heat Sink with Fan
300	17,5		–	–	x
300	17,5	48	2	x	–
366	21,4		–	–	x
366	21,4	40	2	x	–
433	24		–	–	x
433	24	35	2	x	–

The given values were calculated using the formula:

$T_A = T_C - (R_{CA} + R_{GL}) \cdot P$

with P: CPU power dissipation (see table)

R_{CA} Thermal restistant heatsink (see table)

R_{GL} Thermal restistant glue pad (0.35 k/W)

T_C CPU case temperature (85º C)

T_A Air temperature

Table 2—9: Thermal Resistance, Heat Sinks

Air Flow (m/s)	Heat Sink (K/W)	Heat Sink with Fan (K/W)
1	2,8	
2	1,75	
3	1,2	

The maximum air temperature using a CPU fan mainly depends on the long life term of the used fan.The CPU case temperature must not exceed 85º C.

2.2.15 Maximum Operating Humidity:

85% relative (higher value on request)

2.2.16 Power Requirements

Total Power Requirements (without PCI or ISA extensions)

10.0 A max. 7.5 A typ. +5 VDC ±5% (850 MHz)

100 mA max. 30 mA typ. +12 VDC ±10%

100 mA max. 0 mA typ. -12 VDC ±10%

Battery

Type CR 1/3 N, 170 mAh, 3.0 V

Approx. 5 years life term

3 Installation

3.1 Introduction

Do always observe precautions for handling electrostatic devices when unplugging boards from the rack or otherwise handling boards.

Avoid touching integrated circuits except in an electrostatic free environment. Electrostatic discharge can damage circuits or shorten their lifetime.

- Carefully remove the board from the shipping carton.
- Save the original shipping container and packing material for storing or reshipping the board.
- Inspect the board for any shipping damage. If undamaged, the module can be prepared for system installation.
- Set all jumpers to the desired position, refer to Section 2.3 'Jumpers'.

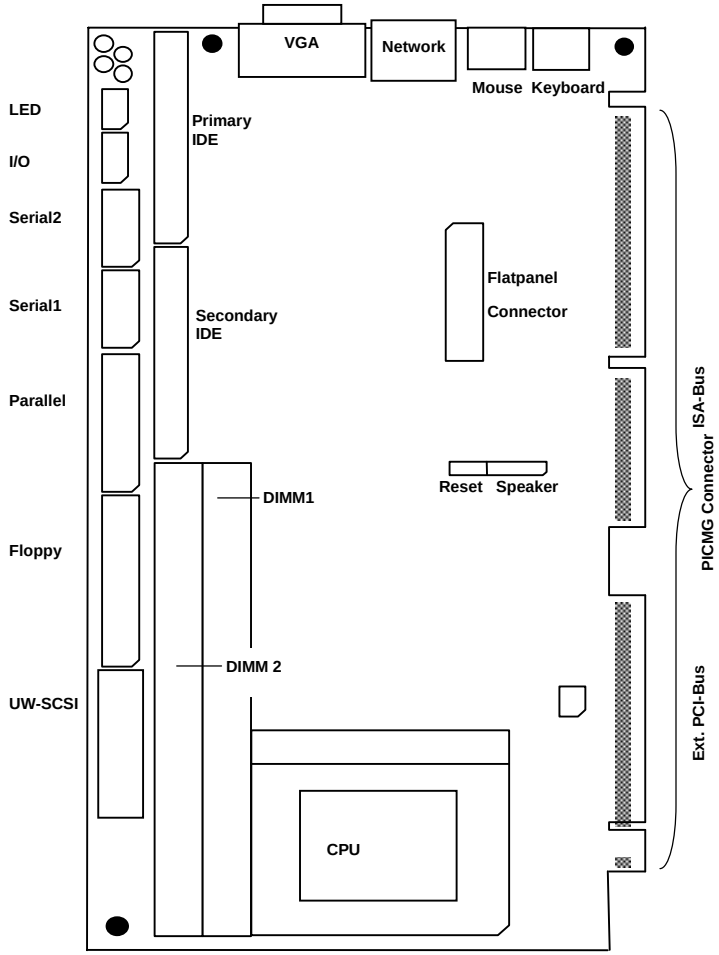

Figure 3—1: Installation Diagram

3.2 DIMM Installation

If the EIPC-3 is not shipped with DRAM DIMMs, the user must insert own DIMMs on the board. The EIPC-3 is not able to run without DRAM.

DIMM installation can be done easily. The board has two DIMM sockets, X401 and X402, representing DRAM bank 0 and bank 1. The BIOS software detects automatically which bank is populated. Also the size of the DIMMs is detected automatically. Also all used DIMMs must have the same speed selection (either 60 or 70 ns access time).

The DIMM is simply plugged into the socket (it fits only in one orientation). The two latches on each socket must hold the DIMM. Otherwise the DIMM is not properly connected.

3.3 Board Installation

The EIPC-3 itself fits into a PICMG CPU slot. Depending on the mounting of the parallel and/or seriell connector the EIPC-3 requires up to 3 slots.After the board was plugged into the PICMG backplane connectors the screw on the front panel can be fixed with the rack. Depending on the housing there may be additional screws and mechanics for fixing the board.

Make sure that the power supply within the rack meets the power requirements specified in Section 'Power Requirements'. Also the operating requirements must meet the values specified in Section 'Environmental Conditions'.

3.3.1 Graphics

If a CRT monitor is used, a standard VGA cable (15 pins) is connected between the monitor and the VGA-connector. Make sure that your monitor is capable of displaying higher video resolutions. If a video mode generates horizontal frequencies much higher than

the maximum value of your monitor, the monitor may be destroyed! If your monitor is not able to display a mode, switch off or disconnect the monitor in advance and select an appropriate video mode for the monitor.

If a flatpanel display should be connected, make sure that the correct display mode is selected in the video BIOS. Check also the connection between the flatpanel connector on the board and the flatpanel display. Please contact ELTEC for further information on supported panel displays and cabling information.

3.3.2 Keyboard

A standard PS/2 keyboard can be connected to keyboard connector

3.3.3 Mouse

A standard PS/2 mouse can be connected to mouse connector.

3.3.4 Parallel Port

A printer with Centronics interface can be connected to the parallel port via the front panel . Other devices with ECC or ECP interface such as a CD-ROM can be connected here as well.

3.3.5 Network

A Network can be connect using 10BaseT or 100BaseTX.

3.3.5.1 External LEDs

These pins can be used to connect external LEDs for HDD and Network activity.

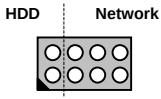

Figure 3—2: Activity LEDs

Table 3—1: Pinout LED Connector

Pin	Name	Function	Function	Name	Pin
1	HDD_ACT	HDD Activity	Power	Vcc	**2**
3	LAN_ACT	Network Activity	Power	Vcc	**4**
5	10Mbit	10Mbit Link	Power	Vcc	**6**
9	100Mbit	100Mit Link	Power	Vcc	**10**

3.3.5.2 Loudspeaker/Reset

These pins can be used to connect a speaker and a reset switch.

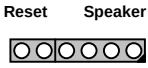

Figure 3—3: Speaker/Reset Connector

Table 3—2: Pinout Speaker/Reset Connector

Pin	Name	Function
1	Speaker	Speaker
2	GND	
3	GND	
4	Vcc	
5	Reset	Reset Switch
6	Reset	

3.3.6 Floppy Disk

The floppy cable is connected between floppy drive and this connector The power supply cable for the floppy drive must be connected directly to the power supply.

Table 3—3: Pinout Floppy Connector

Pin	Name	Name	Pin
1	Gnd	DRVDEN0	**2**
3	Gnd	nc	**4**
5	Gnd	DRVDEN1	**6**
7	Gnd	/INDEX	**8**
9	Gnd	/MTR0	**10**
11	Gnd	/DS1	**12**
13	Gnd	/DS0	**14**
15	Gnd	MTR1	**16**
17	Gnd	/DIR	**18**
19	Gnd	/STEP	**20**
21	Gnd	/WDATA	**22**
23	Gnd	/WGATE	**24**
25	Gnd	/TRK0	**26**
27	Gnd	/WRTPRT	**28**
29	Gnd	/RDATA	**30**
31	Gnd	/HDSEL	**32**
33	Gnd	/DSKCHG	**34**

3.3.7 EIDE

Like the floppy disk drive an IDE drive is connected with its flat cable to these connectors. The power supply cable of the IDE device must be directly connected to the power supply.

Up to two IDE drives (harddisk, CD-ROM) can be connected to each connector. Cable length should not exceed 40 cm to avoid instable operation.

Table 3—4: Pinout EIDE Connectors

Pin	Name	Name	Pin
1	/RST	GND	**2**
3	D7	D8	**4**
5	D6	D9	**6**
7	D5	D10	**8**
9	D4	D11	**10**
11	D3	D12	**12**
13	D2	D13	**14**
15	D1	D14	**16**
17	D0	D15	**18**
19	GND	nc	**20**
21	REQ	GND	**22**
23	/IOW	GND	**24**
25	/IOR	GND	**26**
27	IORDY	nc	**28**
29	/ACK	GND	**30**
31	IRQ14	nc	**32**
33	A1	nc	**34**
35	A0	A2	**36**
37	/CS1	/CS3	**38**
39	/ACT	GND	**40**

3.3.8 SCSI

SCSI is only available on board versions with SCSI option. The SCSI cable is plugged into the appropriate connector on board. All SCSI devices must be cabled in a bus-like fashion, i.e. the cable goes from one device to the next one. The cable end must be terminated to ensure proper operation. An active terminator is recommended. The onboard active terminator has the capability to detect wether onboard termination is neccesary or not. Nevertheless it is possible to select manual termination

Table 3—5: Pinout SCSI Connector

Pin	Name	Name	Pin
1	GND	D12	**2**
3	GND	D13	**4**
5	GND	D14	**6**
7	GND	D15	**8**
9	GND	PD1	**10**
11	GND	D0	**12**
13	GND	D1	**14**
15	GND	D2	**16**
17	GND	D3	**18**
19	GND	D4	**20**
21	GND	D5	**22**
23	GND	D6	**24**
25	GND	D7	**26**
27	GND	PD0	**28**
29	GND	nc	**30**
31	GND	nc	**32**
33	TERMPWR	TERMPWR	**34**
35	TERMPWR	TERMPWR	**36**
37	nc	nc	**38**
39	nc	GND	**40**
41	nc	/ATN	**42**
43	GND	GND	**44**
45	GND	/BSY	**46**
47	GND	/ACK	**48**
49	GND	/RST	**50**
51	nc	/MSG	**52**
53	GND	/SEL	**54**
55	nc	/C_D	**56**
57	GND	/REQ	**58**
59	nc	/I_O	**60**
61	GND	D8	**62**
63	GND	D9	**64**
65	GND	D10	**66**
67	GND	D11	**68**

3.3.9 I/O

This connector contains the one USB- and the IrDA Interface.

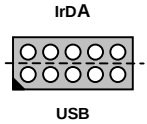

Figure 3—4: USB/IrDA

USB support depends on the operating system. Please contact ELTEC for information about IrDA and USB support.

Table 3—6: Pinout USB/IrDA

Pin	Name	Function	Function	Name	Pin
1	Vcc (USB)	Power	reserved	res.	2
3	USBP0-	USB Data	Vcc (IrDA)	Power	4
5	USBP0+	USB Data	IrDA receive	IrDARx	6
7	GND (USB)	Power	IrDA transmit	IrDATx	8
9	res.	reserved	GND (IrDA)	Power	10

3.4 Replacing the CPU

This section contains information on certified CPU versions for the EIPC-3. Carefully read this section before you are going to replace the CPU on the EIPC-3.

The following information shows CPU versions which have been certified by ELTEC for the different board versions of the EIPC-3. Using CPU versions which have not been certified by ELTEC for the appropriate EIPC-3 board versions, as here displayed may result in damage of both the CPU and the EIPC-3 board. ELTEC takes no responsibility if CPUs are installed in a different way as described here. Misuse will result in loss of warranty.

ELTEC ships all board versions with either a heat sink or a cooling fan. If a CPU is replaced by the same type (same frequency), the same cooling technique must be applied to the replaced CPU. If a heat sink is used, a new glue foil must be used for proper thermal connection between CPU body and heat sink. If a cooling fan is used, the fan must be installed on the CPU the same way as before. If the CPU was replaced by a version with higher frequency (e.g. from 366 MHz to 433 MHz), the cooling technique used currently may not meet the cooling requirements of the installed CPU. In that case ELTEC should be contacted for further information on appropriate cooling techniques. Notice that an inappropriate cooling reduces the reliability of the CPU and may destroy the CPU.

Normally, overclocking of the Celeron or Pentium III processor is not possible.

Table 3—7: Certified CPU Versions

Frequency (MHz)	Intel Order Number	CPU Type
300	FV80524RX300128	Celeron
366	FV80524RX366128	
433	FV80524RX433128	
600	RB80526PY600256	Pentium III
850	RB80526PY850256	

Table 3—8: CPU Fan Connector

Pin	Signal	Function
1	GND	Ground
2	5 V	Vcc
3	Pulse	Fan Pulse Input

4 Jumpers

This section contains a list of jumpers which can be set by the user. Default settings are showing.

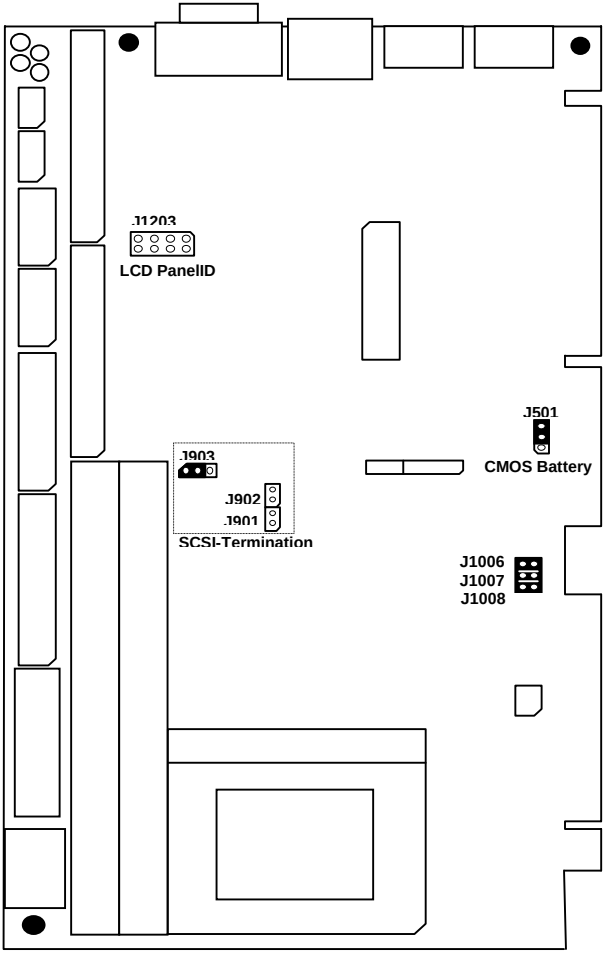

Figure 4—1: Location of Jumpers

4.1.1 CMOS Battery

Table 4—1: Jumper J501

Jumper J501	Function
-	not allowed
1-2	clear CMOS
2-3	normal operation (default)

4.1.2 SCSI-Termination

Table 4—2: Jumper J901-J903

Jumper			
J901	J902	J903	Function
-	1-2	1-2	Automatic Mode (default)
-	1-2	2-3	Automatic LowByte Termination, Enable HighByte Termination
-	1-2	-	Automatic LowByte Termination, Disable HighByte Termination
1-2	1-2	2-3	Enable Termination
1-2	1-2	-	Enable LowByte Termination, Disable HighByte Termination
-	-	-	Disable Termination
all other			not allowed

4.1.3 External PCI Interrupts

There is only one PCI interrupt available for exclusive use on the external bus. Therefore you can select one slot for this interrupt. If your PCI-Device can share ist interrupt with other devices. There is no need changing the default setting.

Table 4—3: Jumper J1006 - J1008

Jumper J1006	Function
1-2	Use IRQ D instead of IRQ A
2-3	default

Jumper J1007	Function
1-2	Use IRQ D instead of IRQ B
2-3	default

Jumper J1008	Function
1-2	Use IRQ D instead of IRQ C
2-3	default

4.1.4 External DMA Routing

If the EIPC-3 comes without a PCI-PCI bridge these jumper configure the routing between internal and external DMA channels. Without a PCI-PCI bridge there a two external DMA channels availiable. Settings may depend on the type of the PICMG backplane. Please refer to backplane documentation before change settings.

Table 4—4: Jumper J1004

Jumper J1202	Function
open	Channel routed to external DMA Channel 0 (default)
1-2	Channel routed to external DMA Channel 1
3-4	Channel routed to external DMA Channel 2
1-2,3-4	Channel routed to external DMA Channel 3

Table 4—5: Jumper J1005

Jumper J1202	Function
open	Channel routed to external DMA Channel 0
1-2	Channel routed to external DMA Channel 1 (default)
3-4	Channel routed to external DMA Channel 2
1-2,3-4	Channel routed to external DMA Channel 3

Note: Same setting for both DMA Channels cause system malefunktion.

4.1.5 LCD Panel ID

Table 4—6: Jumper J1203

Jumper J1203	Panel Type	Dotclock
1-2	Panel 1 : 1024 x 768 DSTN	65 MHz
3-4	Panel 2 : 1280 x 1024 TFT	108 MHz
1-2,3-4	Panel 3 : 640 x 480 DSTN	50 MHz
5-6	Panel 4 : 800 x 600 DSTN	63 MHz
1-2,5-6	Panel 5 : 640 x 480 TFT (Sharp Display)	50 MHz
3,4,5-6	Panel 6 : 640 x 480 TFT (18-Bit)	50 MHz
1-2,3-4,5-6	Panel 7 : 1024 x 768 TFT	53 MHz
7-8	Panel 8 : 800 x 600 TFT	50 MHz
1-2,7-8	Panel 9 : 800 x 600 TFT	40 MHz
3-4,7-8	Panel 10 : 800 x 600 TFT	50 MHz
1-2,3-4,7-8	Panel 11 : 800 x 600 DSTN	40 MHz
5-6,7-8	Panel 12 : 800 x 600 DSTN	40 MHz
1-2,5-6,7-8	Panel 13 : 1024 x 768 TFT	65 MHz
3-4,5-6,7-8	Panel 14 : 1280 x 1024 DSTN	60 MHz
1-2,3-4,5-6,7-8	Panel 15 : 1024 x 600 DSTN	40 MHz
-	Panel 16: 1024 x 600 TFT	50 MHz

5 BIOS Setup

The EIPC-3 is delivered with an AWARD BIOS. The BIOS includes a setup menu to configure basic settings. ELTEC ships the EIPC-3 with optimized BIOS settings. If desired, most of the BIOS settings can be changed (some settings are hardwired). Also if the battery for the CMOS RAM is weak, the RAM may loose its contents making a new setting of the setup necessary. Caution should be taken because some changes of settings may cause an erroneous system behavior.

5.1 Testing the Installation

After power is switched on the BIOS displays a message on the CRT screen. It takes some time before the BIOS is ready to display. After system boot from harddisk or floppy drive the keyboard should work. The driver software for the mouse should detect the mouse device. If a network is installed, other network devices (if existent) should be accessible (e.g from Windows file manager).

6 Programmers Reference

6.1 Memory Address Map

Table 6—1: Memory Address Map

Address Range	Device	Comment
$0000.0000 - $0009.FFFF	640 KB Local DRAM	640 KB lower DRAM
$000A.0000 - $000B.FFFF	128 KB VGA Video Memory	Used for standard VGA modes
$000C.0000 - $000C.7FFF	32 KB Video BIOS EPROM	Video BIOS
$000C.8000 - $000C.BFFF	16 KB SCSI BIOS	If the SCSI controller is disabled via BIOS setup, this range is used by the optional TFT boot BIOS.
$000C.C000 - $000C.FFFF	16 KB BIOS Extension/ PCMCIA	
$000D.0000 - $000D.FFFF	64 KB PCMCIA/ Network EPROM	Reserved for these functions
$000E.0000 - $000F.FFFF	128 KB BIOS	Used by Award BIOS and SCSI
$0010.0000 - $1FFF.FFFF	511 MB Local DRAM	max. 512 MB DRAM
ME[1]- ME+ $0000.00FF	256 B SCSI	SCSI PCI space
ME+ $0080.0000 - ME+ $00FF.FFFF	8 MB VGA	VGA linear video memory

On power-up reset the BIOS is mapped to the address range of 4 GB to 4 GB - 512 KB to read the CPU instruction codes. The BIOS EPROM is not accessible with later cycles at this position.

6.1.1 640KB Local DRAM

This is the lower 640 KB of the complete DRAM. This range is always accessible by the CPU.

[1] ME = End of Mainmemory

6.1.2 128KB VGA Video Memory

The VGA graphics memory occupies segment A and B of the first 1 MB address range. The CPU accesses the video memory in standard videos modes (VGA, CGA). If high resolution video modes are used, video drivers usually access the video memory above the main memory on a 2 MB boundary. The video memory there is accessible in a linear fashion. The complete 1 MB memory is accessible. At power-up the AWARD BIOS maps the video memory above the main memory on the next 2 MB boundary.

6.1.3 32KB Video BIOS EPROM

The lower part of the C segment is reserved for the video BIOS.

6.1.4 16KB SCSI BIOS

If a SCSI device is detected and enabled in the BIOS setup menu, the SCSI BIOS is unpacked and placed in this area. If the SCSI controller is disabled, the optional TFT boot BIOS is placed here.

6.1.5 64KB Network EPROM

The D segment is used by the network boot EPROMs..

6.1.6 128KB BIOS

The E and F segments are exclusively used by the AWARD BIOS and the SCSI extension BIOS.

6.1.7 512MB Local DRAM

The DRAM resides above the first 1 MB. Depending on how much memory is installed up to 511 MB DRAM are accessible.

6.1.8 ISA-Compatible and Power Management Registers

The PCI/ISA bridge contains the ISA-compatible registers which are used for ISA DMA, interrupt and timer functions. Additionally, the bridge contains circuitry for power management. Two registers for generation of PCI configuration cycles are placed within the chipset. All these registers are mainly used by BIOS and device drivers. Please refer to additional PC literature and [2] for details.

Table 6—2: ISA-Compatible and Power Management Registers

I/O Address	Device
$0000-$000F	DMA channel 1
$0020-$0021	**Interrupt controller 1**
$0040-$0043	**Timer counter 1**
$0060-$0061	**NMI control registers**
$0070-$0071	**CMOS RAM and NMI mask registers**
$0080-$008F	**DMA page registers**
$00A0-$00A1	**Interrupt controller 2**
$00B2-$00B3	**Advanced power management controller**
$00C0-$00DF	**DMA channel 2**
$00F0-$00F0	**Coprocessor Error**
$04D0-$04D1	**Interrupt edge level control**
$0CF8	**Configuration address register**
$0CF9	**Reset control**
$0CFC	**Configuration data register**

6.1.9 Local I/O Registers

This list contains a summary of PC related registers which are used for standard I/O purposes like serial, parallel I/O, IDE, floppy disk, graphics controller and keyboard controller. Typically these registers are accessed via BIOS and device drivers. Please refer to additional PC literature for more information.

Table 6—3: Local I/O Registers

I/O Address	Device
$0060-$0064	Keyboard controller
$0170-$0177	IDE secondary command block
$01F0-$01F7	IDE primary command block
$0278-$027F	Parallel port LPTC
$02E8-$02EF	Serial channel 1/2, COM4
$02F8-$02FF	Serial channel 1/2, COM2
$0374-$0377	IDE secondary control block
$0378-$037F	Parallel port LPTB
$0398-$0399	SIO configuration registers
$03B4-$03B5	6845 compatible video controller
$03B8,$03BA	Monochrome register
$03BC-$03BF	Parallel port LPTA
$03C0-$03CF	VGA compatible register
$03D4-$03DA	Color mode register
$03E8-$03EF	Serial channel 1/2, COM3
$03F0-$03F7	Floppy disk controller
$03F4-$03F7	IDE primary control block
$03F8-$03FF	Serial channel 1/2, COM1
$83D0-$83D3	BitBlt offset
$87D0-$87D3	BitBlt pattern
$8BD0-$8BD3	BitBlt background color
$8FD0-$8FD3	BitBlt foreground color
$93D0-$93D3	BitBlt control register
$97D0-$97D3	BitBlt source
$9BD0-$9BD3	BitBlt destination
$9FD0-$9FD3	BitBlt command register
$A3D0-$A3D3	Cursor control
$A7D0-$A7D3	Cursor color 0-1
$ABD0-$ABD3	Cursor color 2-3
$B3D0-$B3D3	Cursor base address
$B7D0-$B7D3	VGA reserved
$BBD0-§BBD3	VGA reserved
$BFD0-§BFD3	VGA reserved

6.1.10 ELTEC-specific I/O Register

The EIPC-3 contains a programmable watchdog trigger. The following register is used for start and trigger of the watchdog.

Table 6—4: ELTEC-Specific I/O Register

I/O Address	Device
$0400-$041F	Watchdog trigger register

6.1.11 Watchdog

The watchdog circuitry is disabled after system reset/power-up. The first write cycle to the watchdog trigger register enables the watchdog. If no further write cycle to this register takes place, the watchdog performs a reset and a new system boot takes place. There is no mechanism to detect a watchdog reset after the system is loaded again. The watchdog trigger must be performed within 200 ms for proper operation.

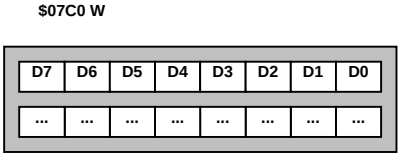

Figure 6—1: Watchdog Trigger Register

Appenix A Reference

[1] PCI-ISA Card Edge Connector, Proposal for single Board Computer (SBC), Rev 2.0, 1994, PCI Industrial Computer Manufacturers Group (PICMG)

[2] 82371AB PCI-TO-ISA/IDE Xcalerator (PIIX), INTEL CORPORATION, 1997, Order Number: 290562-001

Support Request Form

EIPC-3 Revision	
EIPC-3 version:	
Memory size:	
Hardware revision:	
Serial number:	
BSP revision:	
EIPC-3 Configuration	
EIPC-3 IP address:	
Host IP address:	
User name:	
Ftp password:	
Boot file:	
Host Configuration	
Ethernet IP address:	
VxWorks boot file:	
Tornado development tool revision:	
API software revision:	
Operating system and revision:	
Error Description What must be done to reproduce the error:	
Listing of config.h file	

Send the completed form to:
ELTEC Elektronik AG
Support, Mainz/Germany
Phone: +49 (6131) 918-520
Fax: +49 (6131) 918-196
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Web: http://www.eltec.com

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Princeton Forrestal Center
USA-Princeton, NJ 08540-6601
Phone: +1 (609) 4 52 15 55
Fax: +1 (609) 4 52 73 74